Attorney Docket No. 40013.001

EXPRESS MAIL LABEL NO.: EE802420869US
DATE OF DEPOSIT: FEBRUARY 6, 2002

APPLICATION FOR LETTERS PATENT

for

FIELD TRANSISTORS FOR ELECTROSTATIC DISCHARGE PROTECTION AND METHODS FOR FABRICATING THE SAME

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[01] FIELD OF THE INVENTION

[02] The invention generally relates to semiconductor devices and methods for fabricating such devices. More particularly, the invention relates to field transistors for electrostatic discharge protection and methods for fabricating such transistors.

[03] BACKGROUND OF THE INVENTION

[04] To prevent damage to the entire device resulting from electrostatic discharge (ESD) stress, ESD protection circuits are typically coupled to input/output (I/O) terminals or bonding pads or the circuits are positioned in devices susceptible to ESD damage during normal operation of an integrated circuit (IC).

[05] FIG. 1 illustrates a cross-section of a conventional field transistor used for ESD protection. As illustrated in FIG. 1, a p^+-type bottom region 12 and a p-type well region 13 are sequentially formed on a p-type substrate 11. The impurity concentration of the p^+-type bottom region 12 is higher than that of the p-type well region 13. An n^+-type source region 14 and an n^+-type drain region 15 are formed in the p-type well region 13 so that regions 14 and 15 are spaced apart from each other by a distance corresponding to a region for forming an inversion layer. A p^+-type diffusion region 16 is also formed in the p-type well region 13 so that it is spaced apart from the n^+-type source region 14 by a

predetermined distance. The p^+-type diffusion region 16 is provided for applying bias to the p-type well region 13. A field oxide layer 17 is formed on the p-type well region 13 between the p^+-type diffusion region 16 and the n^+-type source region 14 and between the n^+-type source region 14 and the n^+-type drain region 15.

[06] A patterned gate conductive layer 18 is formed on a gate insulating layer 19 and a field oxide layer 17. The gate conductive layer 18 is patterned to overlap parts of the n^+-type source region 14 and the n^+-type drain region 15 while overlapping all of field oxide layer 17. A gate electrode 20 is formed on the patterned gate conductive layer 18. A source electrode 21 is formed so as to contact the n^+-type source region 14 and the p^+-type diffusion region 16. A drain electrode 22, which contacts the n^+-type drain region 15, is connected to the gate electrode 20 in order to apply a turn-on voltage to the gate electrode 20 when ESD stress from the outside is generated through the drain electrode 22. Interlayer dielectric layer 23 is formed and patterned to electrically isolate each electrode.

[07] In the conventional field transistor represented in FIG. 1, when ESD stress from the outside is generated through the drain electrode 22, a turn-on voltage is applied to the gate electrode 20 to form an inversion layer between the n^+-type source region 14 and n^+-type drain region 15. The inversion layer provides a complete current path between a drain terminal and a bulk. Thus, ESD current is routed to the bulk through the n^+-type drain region 15, the inversion layer, the n^+-type source region 14, and the p^+-type diffusion region 16, thereby protecting the devices against the ESD stress.

[08] As depicted in FIG. 1, a gate insulating layer 19 is formed between each of the n^+-type source region 14 and the n^+-type drain region 15 and the gate insulating layer 18 and is significantly thinner than the field oxide layer 17. This smaller thickness increases the possibility of the breakdown of the gate insulating layer 19 due to the ESD stress, significantly reducing the reliability of the device. Such a problem may be solved in two ways. A first way is to make gate insulating layer 19 as thick as the field oxide layer 17. A second way is to form gate conductive layer 18 only on the field oxide layer 17.

[09] The first method is unsatisfactory not only because the manufacturing cost is high, but also the manufacturing process is complicated because of the large number of process steps required by the addition of a mask. The second method is also unsatisfactory in that the n^+-type source region 14 and the n^+-type drain region 15 are not overlapped by the gate conductive layer 18. Thus, even if the inversion layer is formed between the n^+-type source region 14 and the n^+-type drain region 15, the inversion layer is not connected to the source region 14 and drain region 15 and does not providing a complete current path between both regions 14 and 15.

[10] SUMMARY OF THE INVENTION

[11] To solve the above problems, it is a first object of the invention to provide a field transistor for electrostatic discharge (ESD) protection that provides a complete current path between a source and a drain while not using a thin gate insulating layer that is vulnerable to ESD.

[12] It is a second object of the present invention to provide a method of fabricating such a field transistor.

[13] To achieve the first object, the invention provides a field transistor that includes: a well region of a first conductivity type; a field oxide layer for defining an active region on the well region; high concentration source and drain regions of a second conductivity type separated from each other by a width of the field oxide layer; a low concentration source region of the second conductivity type formed in the well region, the low concentration source region being adjacent to the high concentration source region and overlapped by one end of the field oxide layer; a low concentration drain region of the second conductivity type formed in the well region, the low concentration drain region being adjacent to the high concentration drain region and overlapped by the other end of the field oxide layer; and a gate conductive layer formed on the field oxide layer, the gate conductive layer overlapping parts of the low concentration source and drain regions of the second conductivity type.

[14] In one aspect of the invention, the well region of the first conductivity type may be formed on a high concentration buried region of the first conductivity type on a semiconductor substrate of the first conductivity type. Alternatively, in another aspect of the invention, the well region of the first conductivity type may be formed on a semiconductor substrate of the second conductivity type.

[15] In one aspect of the invention, the field transistor further includes a high concentration diffusion region of the first conductivity type formed in the well region, the

high concentration diffusion region being separated from the high concentration source region of the second conductive type by a predetermined distance. In this aspect of the invention, the field transistor may further include a low concentration diffusion region of the first conductivity type and a low concentration diffusion region of the second conductivity type, both low concentration diffusion regions being adjacent to each other between the high concentration diffusion region of the first conductivity type and the high concentration source region of the second conductivity type. The low concentration diffusion region of the first conductivity type can be adjacent to the high concentration diffusion region of the first conductivity type, and the low concentration diffusion region of the second conductivity type can be adjacent to the high concentration source region of the second conductivity type.

[16] In one aspect of the invention, the field transistor further includes: a gate electrode electrically connected to the gate conductive layer pattern; a source electrode electrically connected to the high concentration source region of the second conductivity type; and a drain electrode electrically connected to the high concentration drain region of the second conductivity type. The drain electrode can be electrically connected to the gate electrode and the source electrode can be electrically connected to the high concentration diffusion region of the first conductivity type as well.

[17] To achieve the second object, the invention provides a method of fabricating a field transistor. The method includes: sequentially forming an oxide layer and a mask layer pattern on a well region of a first conductivity type; using the mask layer pattern as

an ion implantation mask to implant impurity ions of the first conductivity type into the well region; forming a photoresist layer pattern on portions of the oxide layer and the mask layer pattern; using the exposed portion of the mask layer pattern and the photoresist layer pattern as an ion implantation mask to implant impurity ions of a second conductivity type into the well region; removing the photoresist layer pattern; forming a field oxide layer in which a portion of the oxide layer is grown using the mask layer pattern as an oxide growth prevention layer while diffusing the impurity ions of the first and second conductivity types to form low concentration source/drain regions of the second conductivity type; forming high concentration source/drain regions of the second conductivity type on either side of the field oxide layer in the well region; forming a high concentration diffusion region of the first conductivity type so that the high concentration diffusion region of the first conductivity type is separated from the high concentration source region of the second conductivity type by a predetermined distance; and forming a gate conductive layer pattern on the field oxide layer.

[18] In one aspect of the invention, the photoresist layer pattern exposes the oxide layer corresponding to a portion of the well region into which the impurity ions of the first conductivity type are implanted. The implantation concentration of the impurity ions of the second conductivity type can be higher than that of the impurity ions of the first conductivity type. The gate conductive layer pattern can overlap the low concentration source/drain regions of the second conductivity type by interposing the field oxide layer therebetween.

[19] In one aspect of the invention, the method further incldues: forming a gate electrode so that the gate electrode is electrically connected to the gate conductive layer pattern; forming a source electrode so that the source electrode is electrically connected to the high concentration source region of the second conductivity type; and forming a drain electrode so that the drain electrode is electrically connected to the high concentration drain region of the second conductivity type. The drain electrode can be electrically connected to the gate electrode and the source electrode can be electrically connected to the high concentration diffusion region of the first conductivity type.

[20] BRIEF DESCRIPTION OF THE DRAWINGS

[21] Figures 1-8 are views of semiconductor devices and methods for making such devices according to the invention, in which:

[22] FIG. 1 illustrates a cross-section of a conventional field transistor for electrostatic discharge (ESD) protection;

[23] FIG. 2 depicts a cross-section of one aspect of a field transistor for ESD protection according to the invention; and

[24] FIGS. 3-8 show cross-section views of various aspects of one method for fabricating a field transistor for ESD protection according to the invention.

[25] Figures 1-8 presented in conjunction with this description are views of only particular—rather than complete—portions of semiconductor devices and methods for making such devices according to the invention.

[26] DETAILED DESCRIPTION OF THE INVENTION

[27] The following description provides specific details in order to provide a thorough understanding of the invention. The skilled artisan will understand, however, that the invention can be practiced without employing these specific details. Indeed, the invention can be practiced by modifying the illustrated devices and methods and can be used in conjunction with devices and methods conventionally used in the industry.

[28] One aspect of the invention is illustrated in FIG. 2, where a p^+-type bottom region 120 and a p-type well region 130 are sequentially stacked on a p-type substrate 110. The impurity concentration of the p^+-type bottom region 120 is higher than those of the p-type substrate 110 and the p-type well region 130. The p^+-type bottom region 120 serves to increase current conduction efficiency in the field transistor, but in one aspect of the invention is not necessary. If the p^+-type bottom region 120 is not formed in the semiconductor devices of the invention, an n-type substrate is used in place of the p-type substrate 110 and the p-type well region 130 is formed in an upper region of the n-type substrate. The n^+-type source region 140 and the n^+-type drain region 150 are formed in the p-type well region 130 so they are separated from each other by a predetermined distance.

[29] An n-type low concentration source region 145, a p-type region 135, and an n-type low concentration drain region 155 are formed between the n^+-type source region 140 and the n^+-type drain region 150 of the p-type well region 130. The impurity concentrations of the n-type low concentration source region 145 and the n-type low concentration drain

region 155 are lower than those of the n^+-type source region 140 and the n^+-type drain region 150, respectively. The impurity concentration of the p-type region 135 is substantially the same as that of the p-type well region 130.

[30] A p^+-type diffusion region 160 is separated from the n^+-type source region 140 by a predetermined distance and is formed in the p-type well region 130. The p^+-type diffusion region 160 is provided for applying bias to the p-type well region 130. A p-type diffusion region 162 and an n-type diffusion region 164 are formed between the p^+-type diffusion region 160 and the n^+-type source region 140. The p^+-type diffusion region 160 is adjacent to the p-type diffusion region 162, and the n-type diffusion region 164 is adjacent to the n^+-type source region 140. The p-type diffusion region 162 is formed adjacent to the n-type diffusion region 164. A field oxide layer 170 is formed between the p^+-type diffusion region 160 and the n^+-type source region 140, i.e., on the surfaces of the p-type diffusion region 162 and the n-type diffusion region 164. The field oxide layer 170 is formed between the n^+-type source region and the n^+-type drain region 150, i.e., on the surfaces of the n-type low concentration source region 145, the p-type region 135, and the n-type low concentration drain region 155.

[31] The patterned gate conductive layer 180 is formed on the field oxide layer 170. While the gate conductive layer pattern 180 does not overlap the n^+-type source region 140 and the n^+-type drain region 150, the entire gate conductive layer pattern 180 overlaps the n-type low concentration source region 145, the p-type region 135, and the n-type low concentration drain region 155. A spacer 190 is formed along the sidewall of

the gate conductive layer pattern 180. A gate electrode 200 is formed on the gate conductive layer pattern 180. A source electrode 210 is formed so that it contacts the n^+-type source region 140 and the p^+-type diffusion region 160. A drain electrode 220, which contacts the n^+-type drain region 150, is connected to the gate electrode 200 in order to apply a turn-on voltage to the gate electrode 200 when ESD stress from the outside is generated through the drain electrode 220. A patterned interlayer dielectric layer 230 for electrically isolating the electrodes from each another is also provided.

[32] The field transistor according to the invention operates in the following manner. When ESD stress from outside of the device of the invention is generated through the drain electrode 220, a turn-on voltage is applied to the gate electrode 200 to form an inversion layer near the top of the p-type region 135. The formation of the inversion layer provides a complete current path between a drain terminal and a bulk. Thus, ESD current is routed to the bulk through the n^+-type drain region 150, the n-type low concentration drain region 155, the inversion layer in the p-type region 135, the n-type low concentration source region 145, the n^+-type source region 140, and the p^+-type diffusion region 160, thereby protecting against the ESD stress.

[33] In the invention, a thin gate insulating layer does not exist in the field transistor. As well, the entire gate conductive layer 180 is formed on the relatively-thick field oxide layer 170. Thus, dielectric destruction of an insulating layer due to the ESD stress does not occur, greatly increasing the reliability of the device. In this aspect of the invention, the n^+-type source/drain regions 140 and 150 are not overlapped by the gate conductive

layer 180. The n-type low concentration source region 145 and the n-type low concentration drain region 155 create a complete current path between the n^+-type source/drain regions 140 and 150. The n-type low concentration source region 145 is formed so that it is adjacent to the n^+-type source region 140 and is overlapped by the gate conductive layer pattern 180 with the field oxide layer 170 therebetween. The n-type low concentration drain region 155 is formed so that it is adjacent to the n^+-type drain region 150 and is overlapped by the gate conductive layer pattern 180 with the field oxide layer 170 therebetween. When the inversion layer is formed at the top of the p-type region, a complete current path is created.

[34] FIGS. 3-8 illustrate cross-sectional views of one aspect of a method of fabricating a field transistor for ESD protection according to the invention. As depicted in FIG. 3, a p^+-type bottom region 120 and a p-type well region 130 are sequentially formed on a p-type substrate 110. The impurity concentration of the p^+-type bottom region 120 is higher than those of the p-type substrate 110 and the p-type well region 130. The p^+-type bottom region 120 may be formed by ion implantation and the p-type well region 130 may be formed by epitaxial growth. However, the methods for forming the p^+-type bottom region 120 and the p-type well region 130 are not limited by these methods.

[35] The p^+-type bottom region 120 serves to increase current conduction efficiency in the field transistor. In one aspect of the invention, the p^+-type bottom region 120 is not formed. In this aspect of the invention, an n-type substrate is used in place of the p-type substrate 110 and the p-type well region 130 is formed in the upper region of the n-type

substrate. In this aspect of the invention, the p-type well region 130 may be formed by ion implantation and/or a drive-in diffusion process.

[36] Next, as illustrated in FIG. 4, an oxide layer 300 and a nitride layer pattern 310 are sequentially formed on the p-type well region 130. Then, an ion implantation process is performed using the nitride layer pattern 310 as an ion implantation mask to partially implant p-type impurity ions into the top of the p-type well region 130.

[37] As depicted in FIG. 5, a mask layer pattern 320 is then formed to cover the desired parts of the nitride layer pattern 310 and the oxide layer 300. An ion implantation process is next performed using the mask layer pattern 320 as an ion implantation mask to partially implant n-type impurity ions into the top of the p-type well region 130. In one aspect of the invention, the implantation concentration of the n-type impurity ions is higher than that of the earlier-implanted p-type impurity ions.

[38] As shown in FIG. 6, a thermal oxidation process is then performed using the nitride layer pattern 310 as an oxidation prevention layer, thereby forming field oxide layer 170. During the thermal oxidation process, a drive-in diffusion process is performed on the implanted p- and n-type impurity ions to form a p-type diffusion region 162, an n-type diffusion region 164, an n-type low concentration source region 145, a p-type region 135, and an n-type low concentration drain region 155. The nitride layer pattern 310 and the oxide layer 300 covered by the nitride layer pattern 310 are removed.

[39] As shown in FIG. 7, any well-known ion implantation process using an ion implantation mask and a drive-in diffusion process are then employed to form a p^+-type diffusion region 160, an n^+-type source region 140, and an n^+-type drain region 150. The ion implantation process is separated into n-type impurity ion implantation and p-type impurity ion implantation, while the drive-in diffusion process is performed so that the n- and p-type impurity ions are simultaneously diffused.

[40] As illustrated in FIG. 8, a gate conductive layer such as a polysilicon layer is formed over the resulting structure of FIG. 7. Then the gate conductive layer is patterned to form a gate conductive layer pattern 180 remaining only on the field oxide layer 170, allowing the edges of the gate conductive layer pattern 180 to overlap the n-type low concentration source region 145 and the n-type low concentration drain region 155, respectively, with the field oxide layer 170 interposed therebetween. Next, a spacer 190 is formed on the sidewall of the gate conductive layer pattern 180.

[41] Subsequently, an interlayer dielectric layer is formed over the resulting structure of FIG. 8. The interlayer dielectric layer is patterned to form the interlayer dielectric layer pattern 230 having openings which partially expose the surfaces of the p^+-type diffusion region 160, the n^+-type source region 140, and the n^+-type drain region 150. Then, as shown in FIG. 2 and known in the art, a metal layer is stacked in the openings to form a source electrode 210 contacting both p^+-type diffusion region 160 and n^+-type source region 140, a gate electrode 200 contacting the gate conductive layer pattern 180, and a drain electrode 220 contacting both n^+-type drain region 150 and gate electrode 200.

[42] In the field transistor and manufacturing method according to the invention, since the entire gate conductive layer pattern 180 is formed only on the field oxide layer 170, there is no relatively thin gate insulating layer (such as layer 19 depicted in FIG. 1). Thus, insulation breakdown of the gate insulating layer due to a strong electric field from the outside is decreased or eliminated, thereby increasing the electrical reliability of the device. Further, the low concentration source/drain regions 145 and 155 adjacent to the source/drain regions 140 and 150, respectively, are overlapped by the edges of the gate conductive layer pattern 180 with the field oxide layer 170 therebetween, forming a complete current path between a drain terminal and a bulk.

[43] Having described the preferred aspects of the invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.